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Qualifying High κ Gate Materials with Charge-Trapping Measurements

Yuegang Zhao, Keithley Instruments, Inc.,

Chadwin D. Young and George Brown, International SEMATECH

Hunting for High k

As the size of transistors continues to scale down, the use of conventional SiO2 as a gate dielectric material is approaching physical and electrical limits [1,2]. The principal limitation is high leakage current due to quantum mechanical tunneling of carriers through the thin gate oxide [3]. To reduce gate leakage current, high dielectric constant (high κ) gate materials, such as HfO_2, ZrO_2 and Al_2O_3 and their silicates [4], have drawn a great deal of attention in recent years. Due to their high dielectric constants, high k gates can be made much thicker than SiO_2 while achieving the same gate capacitance. The result is lower leakage current—sometimes, several orders of magnitude lower.

One of the remaining challenges of deploying high κ materials is reliability. This includes phenomena affecting material reliability, such as voltage breakdown and defect generation mechanisms, and phenomena affecting device reliability, such as hot carrier injection. To characterize the reliability of high κ gate materials fully, multiple measurement techniques are typically required. Usually, these techniques include I-V, C-V, charge-pumping, and other measurements.

Various instruments can be used to take these measurements, but a fully integrated device characterization test system speeds up testing and provides a high level of data integrity. These systems typically integrate source-measure units with a C-V meter and pulse generator to characterize charge-trapping phenomena inside the high κ gate material. They can be used with various charge-trapping measurements, including a relatively new stress and charge-pumping technique that better characterizes traps in high κ films.

Overview of Charge-trapping Measurement Techniques

Charge-trapping techniques involve a series of voltage stresses of certain duration. During voltage stress, leakage current is measured in real time to calculate the amount of charge injected into the gate. This quantity is expressed as:

$$Q_{inj} = \int I_{Leakage} / dt \, .$$

Between voltage stresses, three types of measurements can be done in sequence: C-V, I-V, and charge-pumping. From these measurements, important device parameters can be extracted and plotted as a function of time to show the degradation caused by the stresses.

Stress and C-V Measurements [5]. In this measurement, the device under test (DUT) usually is a MOS capacitor. A C-V sweep is performed on the DUT before and after voltage stress. The C-V sweep can be a full sweep from inversion to accumulation, so that a flat band voltage can be calculated by quantum mechanical modeling. However, a faster and easier way is to do the voltage sweep in a relatively small voltage range around an estimated flat band. The flat band voltage is then extracted from the C-V data. Either a single sweep or bi-directional sweep can be used; a bi-directional sweep will show any hysteresis effects. Flat band voltage as a function of stress time or injected charge provides information on how much charge is trapped in the gate stack structure. The trapped charge may be characterized by an effective value assumed to be located at the insulator-silicon interface (Q_{trap}), given by:

$$Q_{trap} = C_{gate} \cdot \Delta C_{fb} \, .$$

Trapped charge calculated from the change in flat band voltage is an approximation of the charge generated in the semiconductor-insulator interface. However, since charge can be generated in places other than this interface, stress and C-V measurements only give a rough estimate of how much is trapped due to injected charge. (See sample data in ***Figure 1***.)

This measurement technique has the advantage of being simple and direct. It measures the effect of trapped charges from the C-V curve shift along the voltage axis as a function of injected charges. However, it is essential to avoid relaxation of trapped charges during the stress cycle. If trapped charges de-trap too fast, some of the trapped charges may be lost during switching between the stress and C-V measurements. Minimizing the switching time is the key to success in this measurement. Another drawback of this technique is that it measures the combination of traps initially in the film, plus those created later by the stress.

Stress and I-V Measurement. Another method similar to the stress and C-V measurement is stress and I-V measurement on a

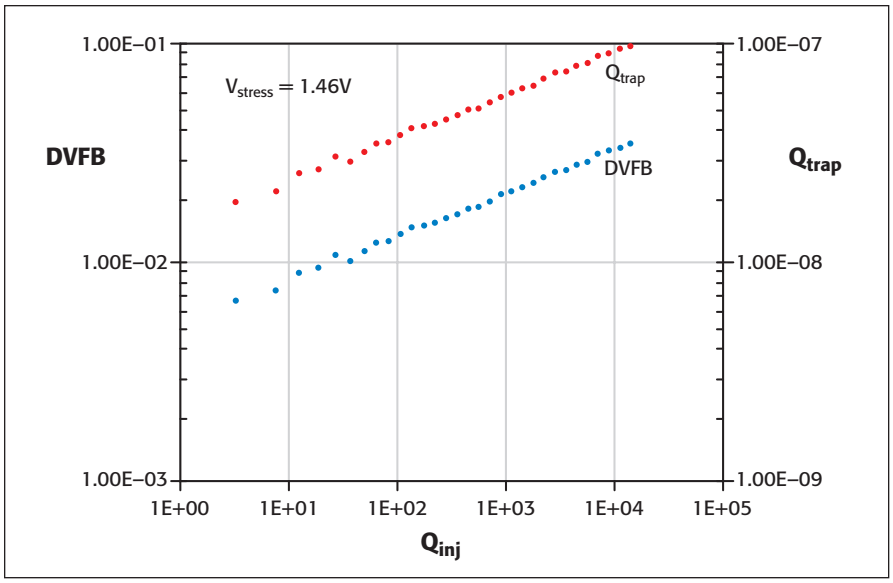

Figure 1. A sample plot of trapped charges and flat band voltage shifts vs. injected charges for HfO_2 film with Equivalent Oxide Thickness = 1.2nm.

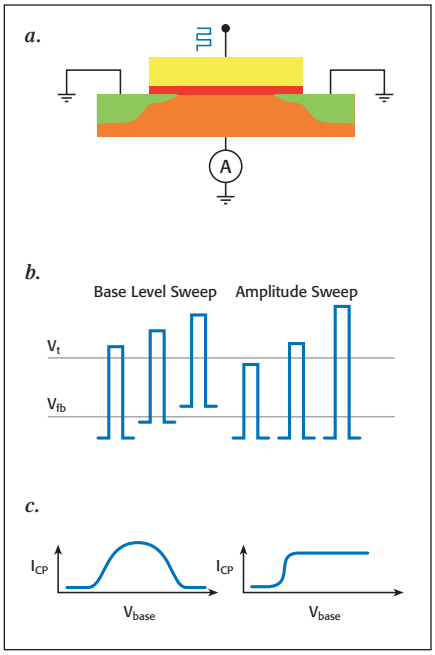

Figure 3. Overview of charge-pumping measurements: (a) Schematic for charge-pumping measurement; source and drain of the transistor are connected to ground; gate is pulsed with fixed frequency and amplitude while body current is measured. (b) Pulse waveform for base voltage sweep; pulse amplitude is constant. (c) Pulse waveform for amplitude sweep; base voltage is constant.

MOSFET. During stress, the source, drain, and substrate terminals are grounded, so that stress is only applied on the gate dielectric. Then, after stress, a V_{gs}-I_d test is performed, so that key parameters, such as threshold voltage and channel transconductance, are extracted. Plotting the shift of those parameters as a function of injected charge makes it possible to obtain the trapped charge density.

This method requires only I-V measurements, so it offers the advantage of being conducted without the need for a switching matrix. This can avoid or significantly reduce charge relaxation effects. However, modeling work is required to interpret the data.

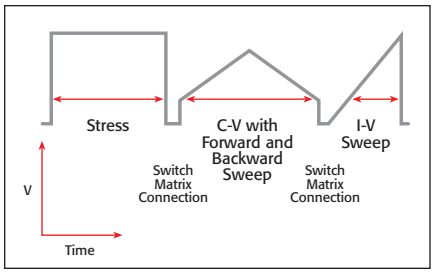

Figure 2. Applied voltage waveform diagram for stress and C-V/I-V measurement.

Figure 2 is an example of voltage waveforms applied to an MIS capacitor in one stress cycle that includes stress, C-V, and I-V measurements. A forward and backward C-V sweep (center waveform in ***Figure 2***) might be used to uncover any hysteresis effect in the high k dielectric film. The instrumentation must be switched from stress to C-V measurement, so a voltage discontinuity appears at the DUT terminals during the switching time. This voltage discontinuity could result in relaxation of trapped charges from trapping centers. If so, the C-V measurement afterwards would indicate a smaller flat-band voltage shift due to fewer trapped charges. Therefore, the switching time between instruments must be minimized.

Charge-Pumping Measurement. Charge-pumping measurements are widely used to characterize interface state densities in MOSFET devices. This type of measurement is especially useful for thin gate materials that have relatively large gate leakage currents when accurate removal of the gate leakage is done [6,7]. Such leakage makes it difficult, if not impossible, to collect simultaneous quasistatic and high frequency C-V measurement data needed to estimate interface state densities. The interfacial-trapped charge (D_{it}) is calculated by:

$$D_{it} = \frac{I_{cp}}{qAf\Delta E},$$

where I_{cp} is the measured charge-pumping current, q is the fundamental electronic charge, A is the area, f is the frequency, and ΔE is the difference between the inversion Fermi level and the accumulation Fermi level [8].

The basic charge-pumping technique involves the measurement of the substrate current while applying voltage pulses of fixed amplitude, rise time, fall time, and frequency to the gate of the transistor with the source, drain, and body tied to ground (***Figure 3a***). The application of the pulse can be done with a fixed amplitude voltage base sweep or with a fixed base variable amplitude sweep.

In a voltage base sweep, the amplitude and period (width) of the pulse are fixed while sweeping the pulse base voltage (***Figure 3b***). At each base voltage, body current can be measured and plotted against base voltage (I_{CP} vs. V_{base}). The interface trap density (D_{it}) as a function of band bending can then be extracted from the charge-pumping current if the ΔE is known.

A fixed base, variable amplitude sweep has a fixed base voltage and pulse frequency with step changes in voltage amplitude (***Figure 3c***). The information obtained is similar to that extracted from a voltage base sweep, but in this case, I_{CP} vs. V_{peak} is plotted. These measurements can also be performed at different frequencies, so that a frequency response of interface traps can be obtained.

For high κ gate stack structures, the CP

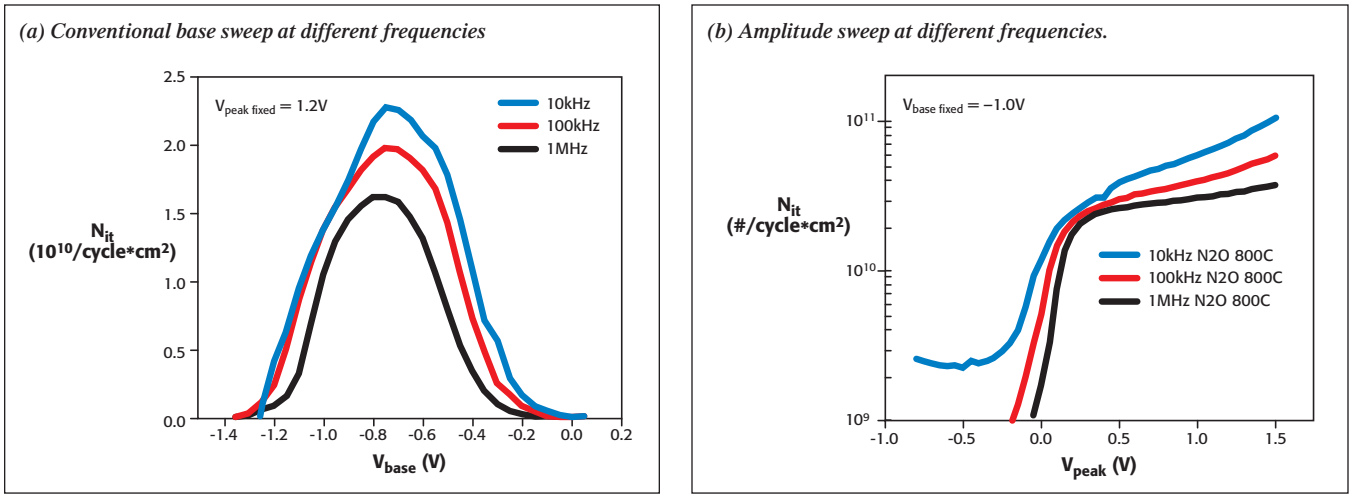

Figure 4. Examples of charge-pumping measurements on MOSFET with high κ gate materials

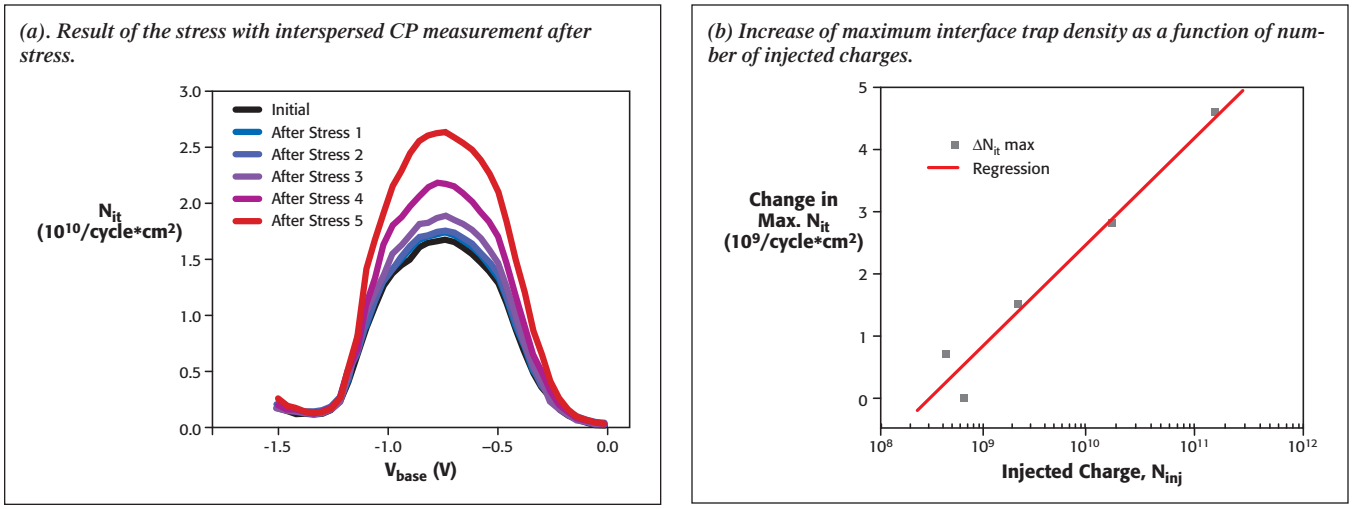

Figure 5. Stress and charge-pumping measurement on a nMOSFET transistor with an ALD HfO_2 gate dielectric and chemical oxide interfacial layer.

technique can quantify the trapped charge (N_{it}) as:

$$N_{it} = \frac{I_{cp}}{qfA,}$$

because trapped charge beyond the silicon substrate/interfacial layer can be sensed [9]. ***Figure 4a*** shows the characteristic N_{it} curve for the base voltage sweep technique, while ***4b*** shows the N_{it} characteristic for the fixed based, variable amplitude technique.

Stress and Charge-Pumping Measurement. Stress C-V, stress I-V, and charge pumping can provide information about charge centers associated with defects already in a gate dielectric film. However, for stress C-V and stress I-V, it isn't possible to distinguish between charge centers initially in the film and those created during a measurement stress cycle. Both types contribute to the shift in flat band voltage during measurements.

However, a recently developed technique can distinguish the initial charge-trapping centers from those created later in the film by voltage stresses. This technique uses a combination of stress and charge-pumping measurements. A major advantage of the new technique is that relaxation of trapped charges during the stress cycle will not affect overall measurement accuracy. The charge-pumping measurements detect traps in high κ gate stacks, so with some modeling work, it is possible to compare results of charge densities before and after a stress cycle. This indicates how many new charge centers were created by injected charges.

Figure 5 shows results from stress charge-pumping measurements on a nMOSFET with W/L = 10/1mm. The gate stack is an ALD HfO_2 with a chemically grown interfacial oxide (EOT) of 1.7nm [10].

Test Hardware Arrangement

The core instrumentation for these measurements is a semiconductor characterization system (SCS) with multiple source-measure units (SMUs) and pre-amps that provide sub-femtoamp resolution for gate leakage currents. This instrumentation is combined with a capacitance measuring instrument, pulse generator, and semiconductor switching matrix for a complete measurement solution. An example of such a system appears in ***Figure 6***. The equipment in this block diagram includes a:

- Keithley Model 4200-SCS Semiconductor Characterization System
- Keithley Model 590 C-V Meter or Agilent Model 4284 LCR Meter

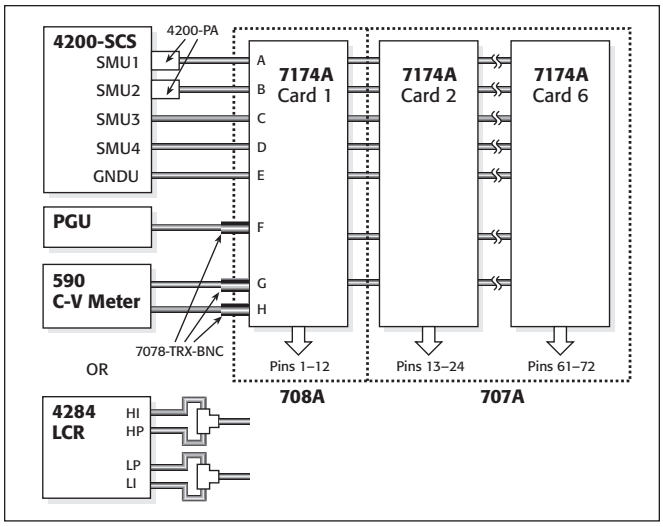

Figure 6. Semiconductor characterization system diagram.

- Agilent 8112 or 8110/81110 Pulse Generator Unit (PGU)
- Keithley Models 707A and 708A switching mainframes with Model 7174A ultra low leakage switch matrix cards

The pulse generator supplies the voltage pulses for charge-pumping measurements. The pulse generator and the C-V meter are connected to the rows of the switch matrix card. DUTs are connected to the columns of the matrix cards. The low leakage and minimal dielectric absorption of the 7174A cards ensure that DUT measurements can be made much faster and more accurately than with general purpose switching cards. The 4200-SCS also has dynamic Trigger Link outputs for control of internal and external instrumentation without using the GPIB, which also speeds up measurements. Its prober drivers provide manual and automatic control of on-wafer measurements.

System Software and Data Communications

For this hardware, the test application is written for use with the Microsoft® Windows® NT operating system running on the PC in the SCS. The software provides test definition, automated control, parameter analysis, and data graphing. Built-in measurement configurations include a sweep mode with nine forcing functions, which reduces programming requirements. Communications between the CPU mainboard and SMUs takes place over a PCI interface, which is much faster than a GPIB interface. This is a key feature in minimizing switching time between stress, C-V, and I-V measurements.

Figure 7 shows two screen captures of the charge-trapping software interface for a test setup and a charge-pumping data plot. To get a complete picture of charge-trapping phenomena in high κ dielectric materials, it's necessary to configure individual tests for all the plausible combinations of stress, C-V, I-V, and charge-pumping measurements. Typical test variables are listed in ***Table 1***. Depending on the SCS, data could be stored in text or Excel format for post-processing. KEITHLEY

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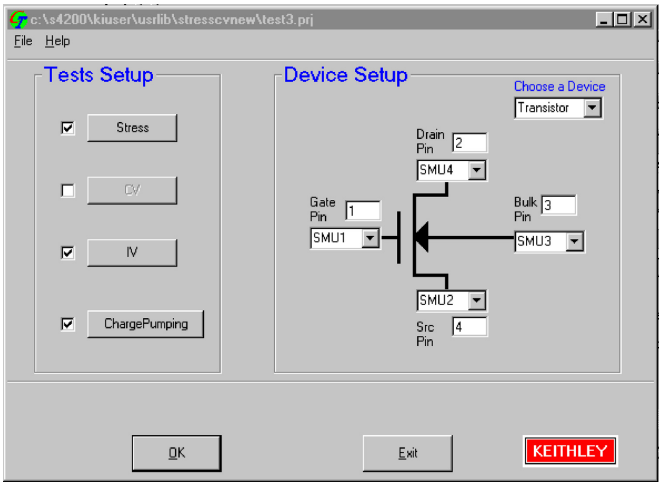

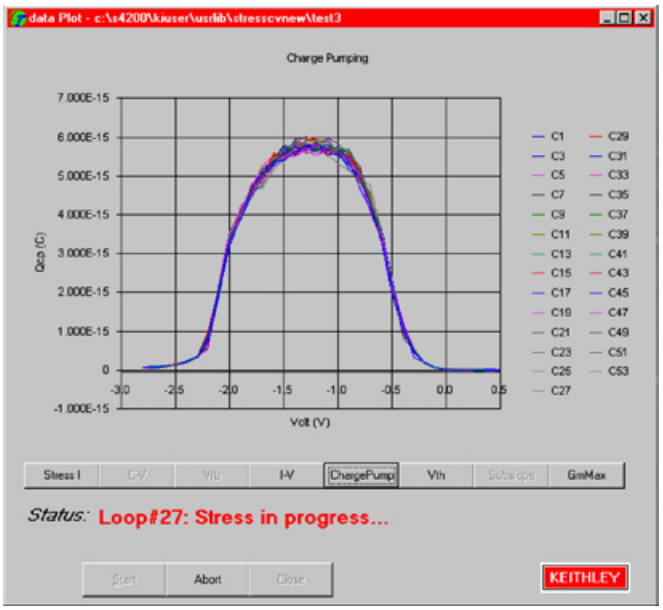

Figure 7. Charge-trapping software interface

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Table 1. List of tests and parameters extracted on charge-trapping test system

Test Type	Stress-Only	Charge Pumping Only	Stress – C-V/I-V	Stress – Charge Pumping
Measurement Performed	Constant Voltage Stress or Voltage-Ramp	Base Voltage Sweep Amplitude Sweep Frequency Sweep	Dual C-V Sweep V_g-I_d Test	Stress and Charge-pumping
Parameters Extracted	TDDB or Q_{BD}*	I_{cp}, Q_{cp}, D_{it}	Shift of V_{fb}, V_t, G_m, sub-threshold slope as function of injected charges	Charge Density, new charge created due to injected charge

* TDDB—Time-Dependent Dielectric Breakdown; Q_{BD}—Charge to Breakdown.

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About the Authors

Yuegang Zhao is a Senior Applications Engineer with the Semiconductor Business Group of Keithley Instruments, Inc. in Cleveland, Ohio. He received his M.S. in Semiconductor Physics from the University of Wisconsin, and his B.S. in Physics from Peking University, Beijing, China. He has five years of experience in semiconductor physics.

Chadwin D. Young is an electrical characterization intern completing his dissertation research in high dielectric constant gate stacks at International SEMATECH in Austin, Texas. He is currently a Ph.D. candidate at North Carolina State University, where he also received an M.S. in electrical engineering. He received his B.S.E.E. from the University of Texas at Austin.

George A. Brown is with International SEMATECH, Inc. as a member of the Front End Processes Research Center, following his recent retirement from Texas Instruments after 37 years of service. He also serves as an industrial resident for the University of Texas, Austin, FEP Research Center projects. He earned a B.S.E.E. from the University of Pennsylvania, and an M.S.E. from Princeton University. He is a member of the IEEE, the Electrochemical Society, and is a section chairman of the ASTM.

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